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09/281,358	03/30/1999	ROGER PANICACCI	08305/031001	7144

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Micron Technology, Inc.  
c/o Tom D'Amico  
Dickstein, Shapiro, Moran & Oshinsky  
2101 L Street, NW  
Washington, DC 20037-1526

EXAMINER
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TRAN, NHAN T

ART UNIT	PAPER NUMBER
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2615

DATE MAILED: 12/19/2003

17

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/281,358

Applicant(s)

PANICACCI, ROGER

Examiner

Nhan T. Tran

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10/6/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1-3 & 8 filed 9/3/2003 have been fully considered but they are not persuasive.

In the last paragraph on pages 8 – 9 of the Amendment, the Applicant asserts that Gowda does not teach or suggest an apparatus wherein “a plurality of analog-to-digital converters ...each of said N logical units having including a plurality of pixels, wherein each analog-to-digital converter includes an ADC portion which receives an analog signal from one of said pixel sensors of an associated logical unit when a selector element associated with said one pixel is enabled, and converts said analog signal to a converted digital value indicating the output signal, and said ADC portion stores said converted digital value into one of a plurality of associated storage elements.” In response, the Examiner respectfully disagrees. As shown by Gowda in Fig. 3 and col. 4, lines 7-12, it is clear that each A/D converter (40) would be tied to multiple column lines. Gowda discloses all the limitations of claim 1 including a plurality of analog-to-digital converters ( $40_1, \dots, 40_N$ )...each of said N columns (e.g.,  $C_1 - C_N$  connected via column lines  $15_1 - 15_N$ ) or N rows (e.g.,  $R_1 - R_M$  connected via  $RSL_1 - RSL_M$ ) including a plurality of pixels (30), wherein each analog-to-digital converter includes an ADC portion (40) which receives an analog signal from one of the pixel sensors of an associated column or row when a selector element (22) associated with one pixel is enabled, and converts the analog signal to a converted digital value indicating the output signal, and the ADC portion stores the converted

Art Unit: 2615

digital value into one of a plurality of associated storage elements ( $42_1, \dots, 42_N$ ) as described in col. 3, line 53 – col. 5, line 8.

Applicant's arguments with respect to claims 4, 5 –7 have been considered but are moot in view of the new ground(s) of rejection based on Gowda et al reference in view of newly cited Kayashi Kazuo reference (JP 06-260938) as analyzed in the following Office Action.

Additionally, in response to the Applicant's arguments with respect to claim 5 stated in the last paragraph on page 9 in which the Applicant asserts that Adiletta fails to teach or suggest the recited limitations of the independent claims, the Examiner respectfully submits it is not necessary for Adiletta to provide all the limitations as recited in the independent claims since the limitations of the independent claims are met by the combination of Gowda and Kazuo except for the limitation of reading of information from an A/D converter unit in a different order than an order in which the information was converted. What is needed is the teaching of big/little endian data format conversion in Adiletta for reading data information in different order in which the information was converted. The teaching of Adiletta has compensated the deficiency in the combination of Gowda and Kazuo as analyzed in the following Office Action.

In view of the above, the Examiner believes that the interpretation of the present claimed invention does, in fact, read on the cited references at least for the reasons discussed above and as stated in the following Office Action.

***Claim Objections***

2. Claim 4 is objected to because of the following reasons:

The claim recites the limitation "said unit storage elements" in lines 3 and 5 on page 4, and the limitation "said information from said second line" in lines 4 and 5 on page 4. There are insufficient antecedent basis for these limitations in the claim. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 3 & 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Gowda et al (US 6,115,066).

Regarding claim 1, Gowda discloses an active pixel sensor comprising:

Art Unit: 2615

an array of pixels, arranged in logical units (columns  $C_1$ - $C_N$ , or rows  $R_1$ - $R_M$ ), wherein each pixel comprises a photosensor element (30), an in-pixel buffer element (25, 23), and in-pixel selector element (22) (see Figs. 3 & 4 and col. 4, line 14 – col. 5, line 8);

a plurality analog-to-digital converters ( $40_1 - 40_N$ ), formed on the same substrate as said pixel sensor array, and each associated with  $N$  logical units of the pixel sensor array (via column lines  $15_1 - 15_N$ ), each of  $N$  logical units having including a plurality of pixels (30) (see Fig. 3 and col. 4, lines 6-13), wherein

each analog-to-digital converter includes an ADC portion (40) which receives an analog signal from one of the pixel sensors of an associated logical unit when a selector element (22) associated with one pixel is enabled, and converts said analog signal to a converted digital value indicating the output signal, and the ADC portion stores the converted digital value into one of a plurality of associated storage elements (42) and  $N$  is at least two (see Fig. 3; col. 3, line 53 – col. 5, line 8, wherein each of the A/D converters would be tied to multiple columns lines 15, therefore  $N = 2, 3, \dots$ ).

Regarding claim 2, the logical units are lines of the array including either columns of the array or rows of the array (see Fig. 3; col. 3, lines 53-64).

Regarding claim 3, Gowda discloses that the analog-to-digital converters are associated with at least two adjacent lines of the array (see col. 4, lines 6-13 for each ADC associated with multiple column lines 15).

Art Unit: 2615

Regarding claim 8, each pixel is a CMOS pixel (see col. 1, lines 19-22).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al (US 6,115,066) in view of Hayashi Kazuo (JP 06-260938) and in further view of Adiletta (US 6,295,546).

Regarding claim 5, Gowda discloses a method for operating a pixel sensor array, comprising:

obtaining a pixel sensor array of photosensitive elements (20), each having photosensitive element in a pixel, a buffer in the pixel (25, 23) associated with the photosensitive element, and a selector transistor in the pixel (22) which is enabled to allow a signal from the pixel to pass, and disabled to block the signal from passing (see Figs. 3 & 4 and col. 4, line 14 – col. 5, line 8);

connecting a plurality of said outputs of said selector transistors to one another, to form a plurality of logical units ( $15_1 - 15_N$ ), each logical unit formed by a plurality of said output transistors (30) which are connected to one another (see Fig. 3);

receiving, in a plurality of A/D converter units (40), respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective first storage units (42) as shown in Fig. 3; col. 3, lines 57-67 and col. 4, lines 6-13, wherein each of the A/D converters 40 would be tied to multiple column lines (15).

Gowda suggests each of the A/D converters 40 to be tied to multiple column lines (15) but Gowda does not provide detailed teaching of multiple registers associated with each A/D converter for separately storing each digital signal corresponding to each pixel of adjacent column lines 15. As taught by Kazuo, it is well known that an A/D converter (1) is connected to a plurality of signal lines (4a - 4n) via corresponding switches (5a - 5n) and the A/D converter is also connected to multiple registers (2a - 2n), wherein the A/D converter sequentially converts signals fed from the signal lines that are controlled by the corresponding switches and separately stores converted signal of each line into its respective register (2a - 2n) for further readout process (see Figs. 5 & 6; paragraphs [0026]-[0028]).

Therefore, it would have been obvious to one of ordinary skill in the art to enable multiple registers associated with each A/D converter in Gowda for sequentially and separately storing digital data converted by the A/D converter corresponding to each pixel of adjacent columns for further readout process in an obvious design variation of an A/D converter with associated registers.

Gowda and Kazuo do not disclose that information in the A/D converters is read out in a different order than an order in which the information was converted. However, Adiletta teaches



Art Unit: 2615

a variation of reading out the digital image information from storage units in either little endian or big endian format for providing an appropriate output conversion format depending upon the requirements of a coupled peripheral multimedia device (see fig. 43B, col. 63, line 55 – col. 64, line 20).

Therefore, it would have been obvious to one of ordinary skill in the art to modify Gowda and Kazuo with Adiletta to provide an alternative reading method from A/D converters in which the digital image information is read out in either little endian or big endian format that is suitable upon requirements of a coupled peripheral device.

Regarding claim 6, the little endian, big endian read out order is in a serial order.

Regarding claim 7, Gowda shows that said units are linear units which are one of rows and columns (see Fig. 3). An Official Notice is taken that it is well known in the art for signal processing to skip lines between conversions in one order, and second order being a complete order in an imaging system.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize a well known feature of skipping lines in signal processing in an imaging system.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al (US 6,115,066) in view of Hayashi Kazuo (JP 06-260938).

Art Unit: 2615

Regarding claim 4, Gowda discloses, a readout controller (14'), controlling readout of information from the photosensor elements, by controlling said analog-to-digital converters (40) to each convert information generated by each pixel from a first line of the array, to store the information from the first line of the array in one of said unit storage elements (42) (see Figs. 3 & 4; col. 3, line 57 – col. 4, line 13). As analyzed in claims 1 and 5 above, Gowda suggests one A/D converter to be tied to multiple column lines but Gowda does not provide detailed description for reading a second line of the array that would be tied to the A/D converter and store information from the second line of the array in the other of unit storage elements, and then to read out the information from all of the unit storage elements in a desired order.

However, as taught by Kazuo, it is well known that an A/D converter (1) is connected to a plurality of signal lines (4a - 4n) via respective switches (5a – 5n) and the A/D converter is also connected to multiple registers (2a – 2n), wherein the A/D converter sequentially converts signals fed from the signal lines that are controlled by the corresponding switches and separately stores converted signal of each line into its respective register (2a – 2n) for further readout process (see Figs. 5 & 6; paragraphs [0026]-[0028]).

Therefore, it would have been obvious to one of ordinary skill in the art to enable multiple registers associated with each A/D converter in Gowda for sequentially and separately storing digital signal converted by the A/D converter corresponding to signal information from adjacent columns and then perform readout of all signal information from all register in a desired order in an obvious design variation.

It is also noted that readout of signal information in a desired order is inherent in all imaging systems.

Art Unit: 2615

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NT.



ANDREW CHRISTENSEN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600